XpressGX5LP-SE

Reference Manual

Version 1.0.0 November 2013

XpressGX5LP-SE

Reference Manual

Document Change History

Date	Doc Version	Board Version	Change
November 2013	1.0.0	P128 v1.0.0	• First release

Proprietary Notice

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Preface

About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA XpressGX5LP-SE board. Prior knowledge of PCI Express is assumed.

Additional Reading

PLDA periodically updates its documentation. Please contact PLDA Technical Support or check the Web site at http://www.plda.com for current versions.

Please refer to the following documents for information on specification standards:

- *PCI Express™ Specification, Revision 2.0*
- *PCI Express Card Electromechanical Specification, Revision 2.0*

Feedback and Contact Information

Feedback about this document

PLDA welcomes comments and suggestions about this documentation. Please contact PLDA Technical Support and provide the following information:

- the title of the document
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- a description of your comments

Contact information

Corporate Headquarters

PLDA
Parc club du golf - Bât. 11a
Rue Guillibert
13856 Aix-en-Provence Cedex 3 - France

Tel: USA +1 408 273 4528 - International +33 442 393 600
Fax: +33 442 394 902

http://www.plda.com

Sales

For sales questions, please contact sales@plda.com.

Technical Support

For technical support questions, please contact PLDA Support at http://www.plda.com/plda_login.php using the Support Center if you have a PLDA online account.

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Chapter 1 Introduction

1.1 Purpose of the Board

The XpressGX5LP-SE board is designed to enable all engineers, even those with little PCI Express experience, to design complex applications using PCIe and 10 Gigabit Ethernet as their main communication interfaces.

XpressGX5LP-SE is a low-profile, highly-integrated PCI Express FPGA board with two fully independent 10 G Ethernet channels engineered for both prototyping and field deployment.

The board is based on the Altera Stratix V GX in the FBGA 1517 package and is available with either the 5SGXEA7K2F40C2N or the 5SGXEA4K2F40C2N FPGA.

1.2 Features List

- PCI Express x8 2.5/5.0/8.0 Gbps (Gen 1, 2 or 3)
  - PCI Express edge connector
- .Dual 1G/10G ethernet channels
  - Two SFP+ interfaces to support 2 independent protocols on fiber optic or copper tranceivers.
- Stratix V GX FPGA
  - 5SGXEA7K2F40C2N or 5SGXEA4K2F40C2N
- Board configuration module
  - Power monitoring
    - Power-Up and reset controller
  - IP protection (PLDA Protocore)
  - FPGA configuration functionality supports
    - Complete FPGA configuration from Flash Devices
    - Flash image boot management
    - FPGA re-load functionality
- Clock circuitry
  - FPGA configuration (Flash): 40 MHz
  - PCIe: 100 MHz
  - 1G/10G: 644.53125MHz Clock
  - DDR3 & QDR2+ SRAM: 200 MHz
- Memories
  - Two 4 GB DDR3L-1600 SDRAM with 72-bit data path (2x8GB capable)
  - Two 144Mbit QDR2 + SRAM with 18-bit data path
  - 256 or 512 MB Flash
  - Two 256Kbit I2C EEPROMs
- Extension Serial link
  - Board capabilities extension or board-to-board connection over SAMTEC QSH connector (optional)
- General I/Os
  - Eight user LEDs
  - Four FPGA configuration LEDs
  - Four tri-color LEDs on the board bracket
  - One reset button
  - One FPGA configuration reload button
  - One FPGA image boot selector
  - Three user switches
  - Board-to-board Interface (4 GXB Rx/Tx + 10 LVCMOS) (optional)
- Power supply

- PCI Express edge connector power (12 V and 3.3 V)
  - Power derived directly from PCI Express slot
- Mechanical
  - Low profile PCI Express height

A detailed description of board features can be found in Section 2.3.

1.3 System Requirements

To use XpressGX5LP-SE board features, you must install the **PLDA Software Tools**. The PLDA Software Tools can be downloaded from PLDA's extranet site. You can log in to the extranet from PLDA's web site www.plda.com.

1.4 Board Configuration Requirements

- Altera USB-Blaster
- Altera Quartus 12.1 SP2 dp7

Chapter 2 XpressGX5LP-SE Architecture

The XpressGX5LP-SE board is supplied by both the 12 V and 3.3 V of the PCI Express slot. The PCI Express 12 V generates 1.35 V, 1.8 V, 2.5 V, and 0.9 V voltages, while the 3.3 V generates 3.0 V voltages.

These voltages are available on the mezzanine power supply daughter card, which is mounted on the XpressGX5LP-SE by default. This daughter card is supplied with the XpressGX5LP-SE board. See Section 3.13 for more information.

The XpressGX5LP-SE is delivered with a fansink mounted on the FPGA.

2.1 XpressGX5LP-SE Layout

The following figure shows the component side of the XpressGX5LP-SE board with the mezzanine power supply daughter card:

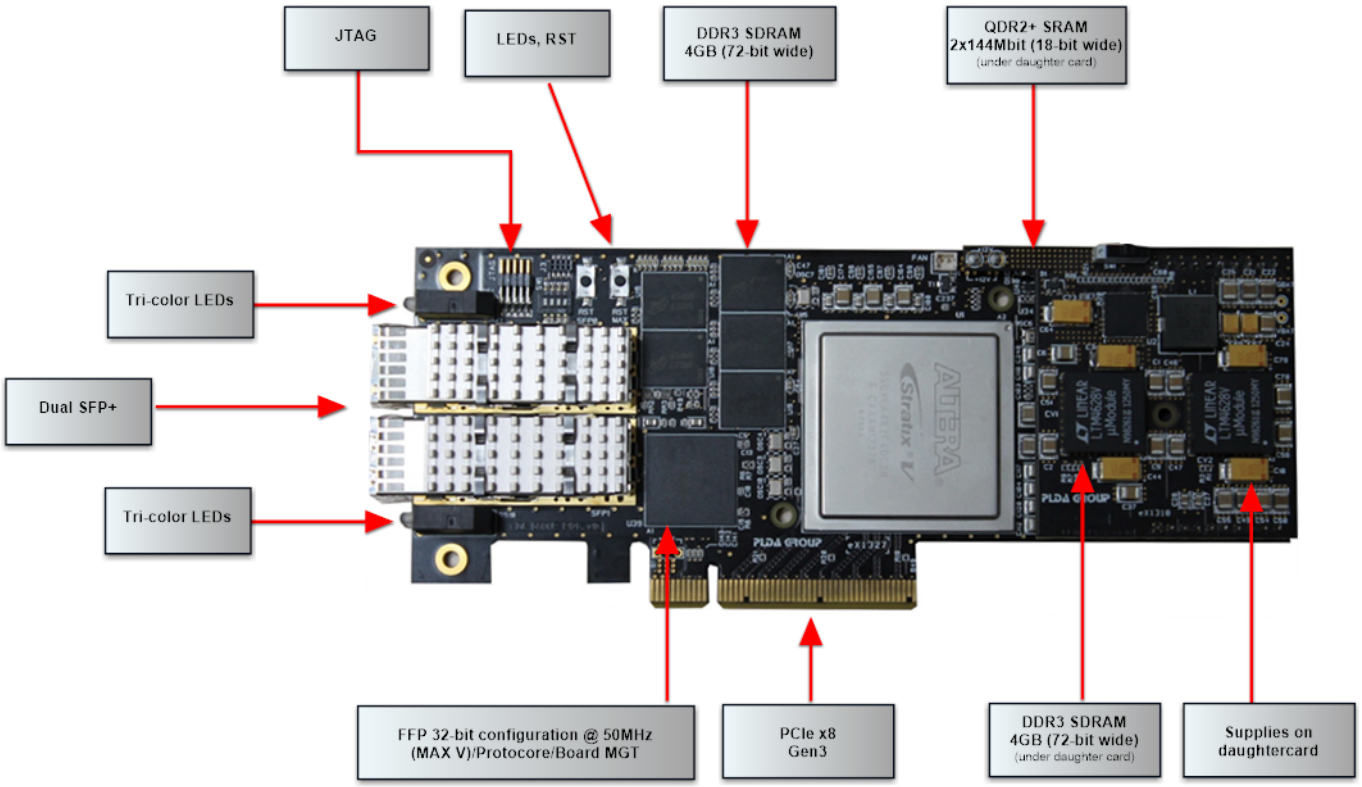

Figure 1: XpressGX5LP-SE layout

2.2 Block Diagram of the Board

The XpressGX5LP-SE board is based on an Altera Stratix V GX FPGA, as shown below:

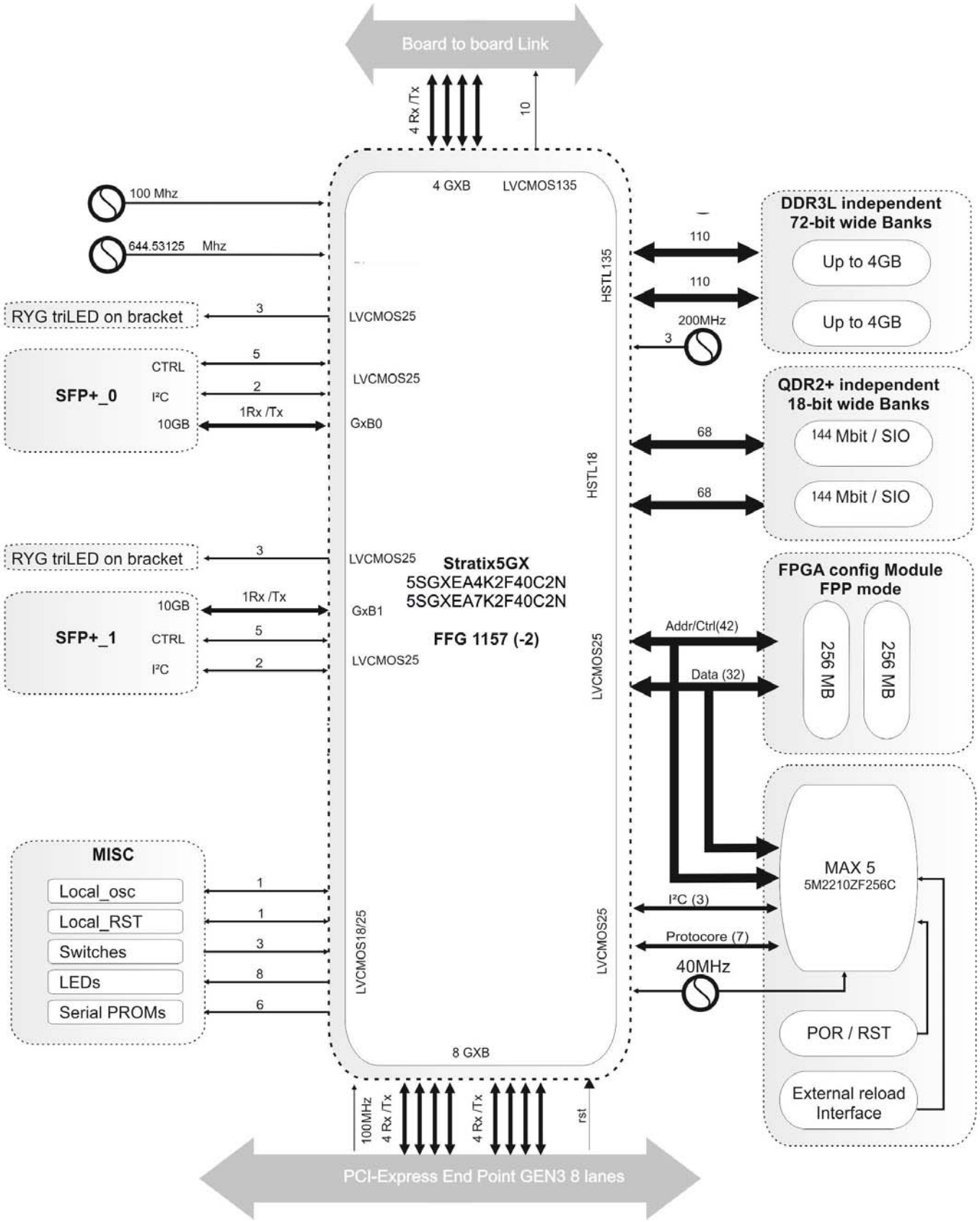

Figure 2: XpressGX5LP-SE block diagram

2.3 Board Features

The following table describes XpressGX5LP-SE board features:

Feature name	Description	For more information, see ...
x8 PCI Express 3.0 male connector	This connector supports PCI Express at 2.5, 5.0, and 8.0 Gbps for x8, x4, and x1 link width. PCI Express is provided via FPGA transceivers.	Section 3.4
Dual SFP+ interfaces	Two independent SFP+ interfaces using two GxB on the FPGA to enable two 1/10 (or other data rate) links.	Section 3.7
QDR2+ SRAM	Two independant QDR2+ SRAMchips are available, which feature: • 144Mbit density • 18-bit data path • separate IO • 400MHz clock Frequency	Section 3.5
DDR3 SDRAM	Two independent banks of DDR3L-SDRAM are available. Each bank consists of 9 x 4 Gb (8-bit wide) chips, which feature: • Up to 8 Gbytes density (4 Gbytes are mounted by default) • 72-bit data path • Up to 800 MHz clock frequency • Maximum throughput of 12.8 Gbytes per bank	Section 3.6
Extension serial link	The extension serial link uses four Rx/Tx Gigabit links to enable board-to-board data transfer of up to 40 Gbps. This link also provides ten other LVCMOS signals.	--
Board configuration module	A 32-bit configuration module (40MHz) is available to configure the FPGA at each board power-up. This module consists of two 2-Gbit Numonyx Flash Devices and an Altera MAX V The Flash devices can be programmed using PLDA's FlashPCI software. Each device is directly connected to the FPGA and the CPLD pins.	Section 3.2
JTAG connector	A mini JTAG connector is available on the board. You must use the extender provided by PLDA to configure the FPGA via JTAG, using an Altera USB-Blaster and Quartus.	
Max V Board Manager	The on board MAX V CPLD manages FPGA configuration, as well as IP protection, CvP, partial reconfiguration and power/temperature management.	
Reset button	1 local power-on reset button on the component side of the board.	Section 3.10
Switches	3 micro switches on the component side.	Section 3.11
Tri-color LEDs	Two dual tri-color LEDs are available on the board bracket and can be used to display information about the SFP+ connectors or user-defined information.	Section 3.8
LEDs	8 user LEDs are available on the component side of the board.	Section 3.9
EEPROMs	Two 256k-bit Serial FlashPROMs are available for data storage via two I²C links	Section 3.12
Power supply	Power is provided via a daughter card supplied by the PCIe slot (12/3.3 V).	Section 3.13

Table 1: Board features description

2.4 Mechanical Description

The following diagram illustrates the mechanical architecture of the XpressGX5LP-SE board without the fansink mounted.

Note: The overall height of the board, that is, the height of the highest component, is 14mm.

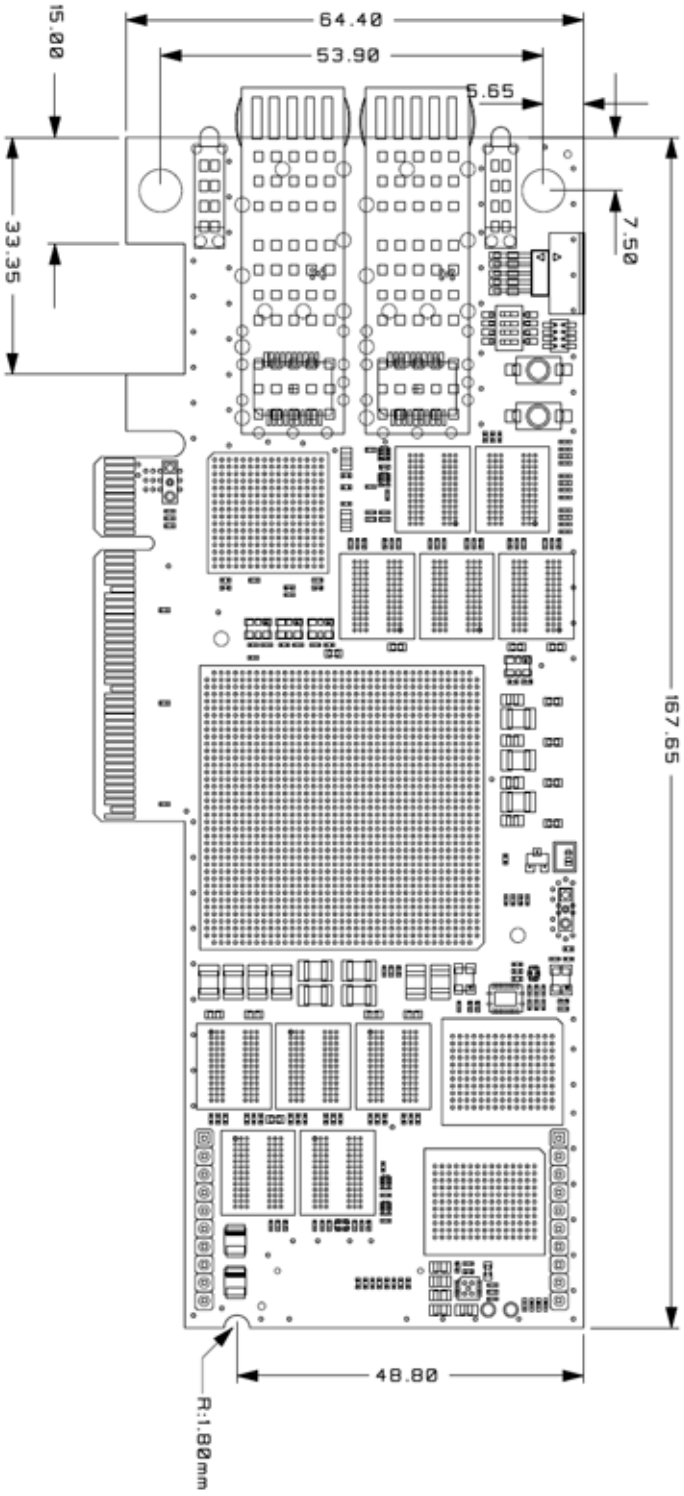

Figure 3: XpressGX5LP-SE component side with daughter card

Chapter 3 XpressGX5LP-SE Features

3.1 Stratix V GX FPGA Device

The XpressGX5LP-SE board can be mounted with either the Altera 5SGXEA7K2F40C2N or the 5SGXEA4K2F40C2N FPGA. The following table shows the resources of each available Stratix V GX FPGA:

FPGA	LEs	Registers	M20K RAM Blocks	M20K Memory	18x18 Multipliers	27x27 Multipliers	PLL
5SGXA4	420 K	634 K	1900	37 Mbits	512	512	24
5SGXA7	622 K	939 K	2560	50 Mbits	256	256	28

Table 2: Stratix V GX FPGA Resources

3.2 Board Configuration Module

3.2.1 JTAG

The XpressGX5LP-SE features a mini JTAG connector. A 10cm cable is provided with the board so you can configure the FPGA with your USB-BLASTER and Quartus.

The cable must be plugged into the board as shown in the following picture:

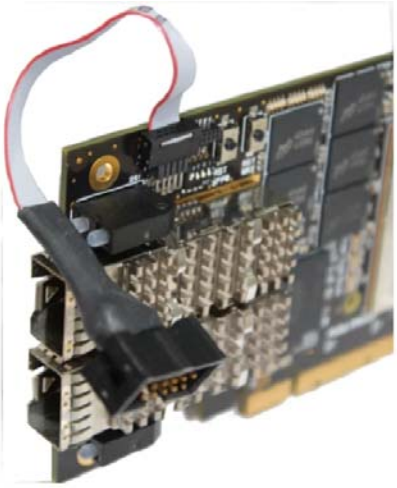

Figure 4: JTAG Connector

3.2.2 FlashPROM Configuration

The XpressGX5LP-SE uses an Altera 5M2210ZF256C5N MAX V CPLD as a 32-bit FPP configuration module.

This module consists of two 256MB PC28F00BP30EFA Micron 16-bit FlashPROMs that are directly connected to the FPGA on the FPP configuration interface.

At power-up, the CPLD acts as an address counter to configure the FPGA.

Both FlashPROMs are accessible via the FPGA and the CPLD (data, address and control signals are shared between these devices).

Switch (SW1-4) is available to select a boot sector (0 or 1).

The following figure shows the configuration components of the XpressGX5LP-SE:

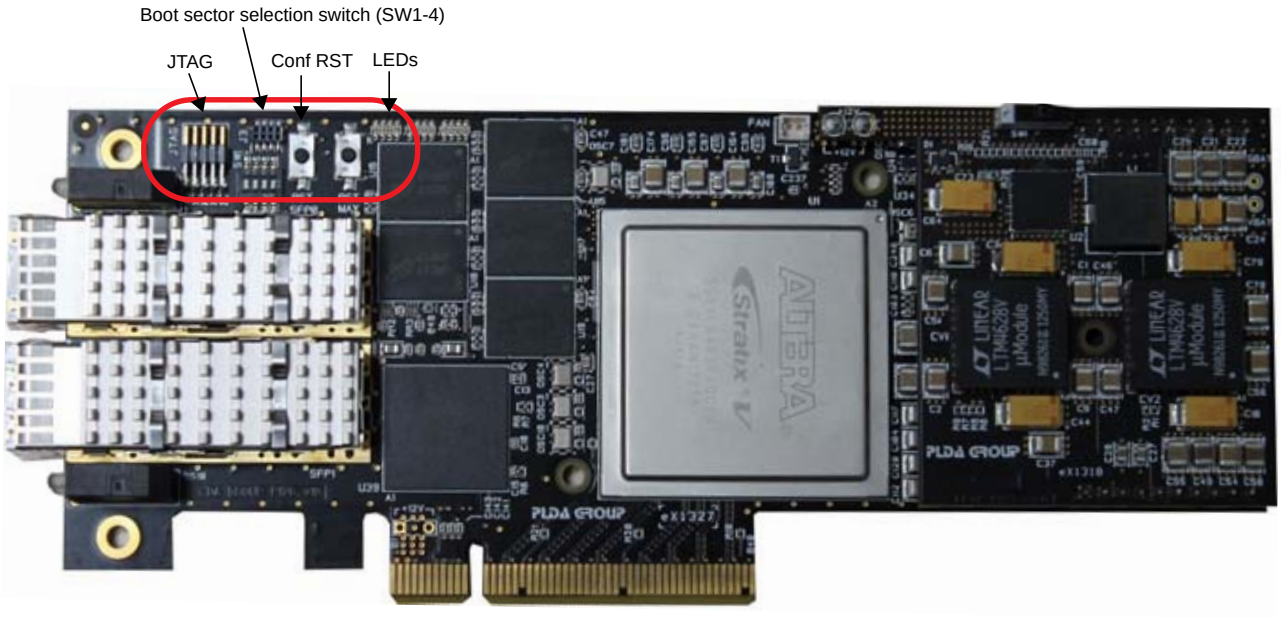

Figure 5: Board configuration components

The following diagram shows the board configuration module:

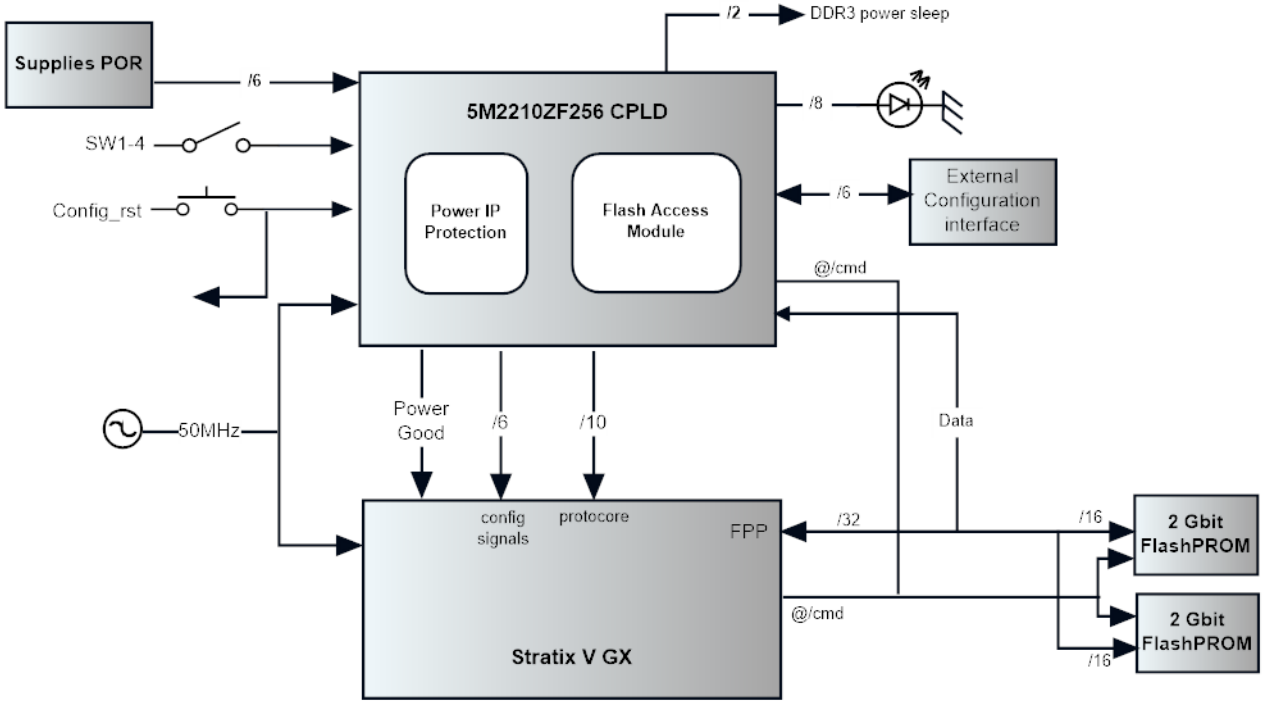

Figure 6: Max V 5M2210ZF256 board configuration and management module

The following table shows pin assignments for the FlashPROM:

Flash Data	FPGA	CPLD	Flash Address	FPGA	CPLD	Flash Control Signal	FPGA	CPLD
flash_data00	AP33	B12	flash_ad00	AJ29	K2	flash1_adv#	AK26	B9
flash_data01	AT33	C12	flash_ad01	AK30	N1	flash1_ce#	AL26	D10
flash_data02	AR33	B16	flash_ad02	AW23	P2	flash1_oe#	AM25	A10
flash_data03	AU34	C11	flash_ad03	AU23	M3	flash1_rst#	AN25	C10
flash_data04	AU33	D11	flash_ad04	AP25	M4	flash1_wait	AN24	C9
flash_data05	AN31	B14	flash_ad05	AK29	K3	flash1_we#	AL25	A9
flash_data06	AM31	A11	flash_ad06	AR25	N2	flash1_wp#	AN26	E10
flash_data07	AU32	A13	flash_ad07	AL30	J1	--	--	--
flash_data08	AT32	B10	flash_ad08	AL29	L1	flash2_adv#	AL27	B3
flash_data09	AR31	D12	flash_ad09	AV25	N3	flash2_ce#	AL28	C4
flash_data10	AP31	C13	flash_ad10	AU24	L4	flash2_oe#	AN28	A4
flash_data11	AW34	B13	flash_ad11	AW25	M2	flash2_rst#	AM28	C3
flash_data12	AV34	B11	flash_ad12	AP27	J2	flash2_wait	AK27	B1
flash_data13	AW31	A15	flash_ad13	AU26	L2	flash2_we#	AN27	A2
flash_data14	AV31	A12	flash_ad14	AU25	M1	flash2_wp#	AJ27	C2
flash_data15	AW32	E11	flash_ad15	AV26	L5	--	--	--
flash_data16	AV32	E6	flash_ad16	AW26	K5	flash_clk	AM26	B4
flash_data17	AJ33	F5	flash_ad17	AP28	G1	--	--	--
flash_data18	AH33	F6	flash_ad18	AR27	G2	--	--	--
flash_data19	AL33	G3	flash_ad19	AT26	H2	--	--	--
flash_data20	AK33	D1	flash_ad20	AU27	L3	--	--	--
flash_data21	AK32	E5	flash_ad21	AM29	F4	--	--	--
flash_data22	AJ32	D3	flash_ad22	AT24	J3	--	--	--
flash_data23	AH31	C8	flash_ad23	AV23	K4	--	--	--
flash_data24	AG31	G4	flash_ad24	AT27	H1	--	--	--
flash_data25	AF31	G5	flash_ad25	AR28	F3	--	--	--
flash_data26	AE31	E7	flash_ad26	AT23	H3	--	--	--
flash_data27	AJ30	E3	--	--	--	--	--	
flash_data28	AH30	E2	--	--	--	--	--	
flash_data29	AR30	D8	--	--	--	--	--	
flash_data30	AP30	D2	--	--	--	--	--	
flash_data31	AU30	E1	--	--	--	--	--	

Table 3: FlashPROM pin assignments

The following table shows the pin assignments for the FPGA and CPLD configuration signals:

FPGA Configuration Signals			
Signal	**CPLD**	**Signal Name/Function**	**FPGA**
nConfig	K13	nConfig	AK35
Conf_done	K15	Conf_done	AH6
Nstatus	L15	nstatus	AM5
Init_done	K12	Init_done	AL34
Dclk_cpld	J4	Dclk_CPLD	AC31
Msel0	H14	Msel0	AA9
Msel1	G14	Msel1	AA10
Msel2	H15	Msel2	AD8
Msel3	G15	Msel3	AG8
Msel4	H16	Msel4	AH7
CPLD Configuration Signals			
osc_config_cpld	H5	osc_config_fpga	AV29
clrconfig#	E14	Reset push button (BPCONF)	--
Max_SW0	C14	Configuration boot sector switch (SW1-4)	--
flash_reload_enable (conf_rfu0)	L14	Flash reload enable	AV22
flash_boot_number (conf_rfu1)	N14	Flash boot number	AR24
Conf_rfu2	K14	Conf_rfu2	AR22
conf_rfu3	J14	conf_rfu3	AU21
conf_rfu4	N15	conf_rfu4	AM23
conf_rfu5	M15	conf_rfu5	AW22
conf_rfu6	M14	conf_rfu6	AP24
CPLD Configuration LEDs			
cpld_confdone	R13	CPLDOK LED (green)	--
max_leduser0	R14	DSMAX0 LED (Red)	--
max_leduser1	T15	DSMAX1 LED (Green)	--
max_leduser2	R16	DSMAX2 LED (Orange)	--
XpressGX5LP-SE Power Management			
ddr3_pgood	D4	DDR3 termination supply power good	--
ddr3_slp_s3	D6	DDR3 termination supply enable	--
por_VCCA_GXB	N10	VCCA_GXB Power on Reset	--

Table 4: FPGA and CPLD pin assignments

FPGA Configuration Signals			
Signal	**CPLD**	**Signal Name/Function**	**FPGA**
por_VCCR_GXB	F14	VCCR_GXB Power on Reset	--
fpga_power_good	F15	FPGA power good	AC25
Protocore Dedicated Signals			
prot0_out	G13	prot0_out	AG26
prot1_in0	E12	prot1_in0	AE25
prot1_in1	E13	prot1_in1	AF23
prot1_out	F12	prot1_out	AE24
prot2_in0	H13	prot2_in0	AG24
prot2_in1	G12	prot2_in1	AE23
prot2_out	F13	prot2_out	AJ26
fpga_proto_misc0	A5	fpga_proto_misc0	AB27
fpga_proto_misc1	A7	fpga_proto_misc1	AA26
fpga_proto_misc2	C7	fpga_proto_misc2	AC26
fpga_proto_misc3	B6	fpga_proto_misc3	AA27
fpga_proto_misc4	A6	fpga_proto_misc4	AC27
fpga_proto_misc5	B7	fpga_proto_misc5	AD26
proto_led0	M11	DSMAX3 LED (Red)	--
proto_led1	M12	DSMAX4 LED (Green)	--
proto_led2	M7	DSMAX5 LED (Orange)	--
proto_led3	M6	DSMAX6 LED (Green)	--
XpressGX5LP-SE Temp MGT			
--	--	fpga_temp_n (LM83)	P5
--	--	fpga_temp_p (LM83)	R6
smb_temp_clk	N8	LM83 (U38.14)	--
smb_temp_d	P12	LM83 (U38.12)	--
temp_crit#	N9	LM83 (U38.16)	--
temp_int#	T12	LM83 (U38.11)	--
External Configuration Management Interface (on J3 Connector)			
External_CPLD_IF_0	D13	TBD (pin J3.1]	--
External_CPLD_IF_1	D16	TBD (pin J3.3]	--
External_CPLD_IF_2	D14	TBD (pin J3.5]	--
External_CPLD_IF_3	E15	TBD (pin J3.7]	--
External_CPLD_IF_4	E16	TBD (pin J3.4]	--
External_CPLD_IF_5	D15	TBD (pin J3.6]	--

Table 4: FPGA and CPLD pin assignments

FPGA Configuration Signals			
Signal	**CPLD**	**Signal Name/Function**	**FPGA**
CvP / PR signals (Configuration via protocol / Partial reconfiguration			
Cvp_confdone	M13	Cvp_confdone	AT29
pr_done	L12	pr_done	AT30
pr_error	N13	pr_error	AU29
pr_ready	L11	pr_ready	AN29
pr_request	L13	pr_request	AN30

Table 4: FPGA and CPLD pin assignments

The following table shows the memory mapping for the Flash Access Module:

Name	Size	Address
FPGA Sector 1 or User Sector (SW1-4 = 1)	64MB	7FF FFFF 400 0000
Sector 0 (SW1-4 = 0)	64MB	3FF FFFF 000 0000

Table 5: Flash Memory Mapping

3.3 Dedicated Clocks

The following table describes clock assignments for the board:

Signal	FPGA Pin	Type	Comment
osc_config_FPGA	AV29	LVCMOS25	Single-ended 40MHz clock used for the Max V CPLDs.
Osc3 p/n	AK23/AL23	LVDS	125 MHz CLK used for PCIe Hard IP
Osc4p/n	AE17/AE16	LVDS	100MHz CLK for global CLK network
Osc5 p/n	E34/D34	LVDS	200 MHz CLK dedicated to DDR3L Bank1
Osc7 p/n	AV7/AW7	LVDS	200 MHz CLK dedicated to DDR3L Bank0
Osc8 p/n	J23/J24	LVDS	200 MHz CLK dedicated to QDR2 banks
Gxb Transceiver Clock inputs			
Pcie_clk_100MHz p/n	AF34/AF35	HCSL	100 MHz Transceiver RefCLK for PCIe Gen2

Table 6: XpressGX5LP-SE clock assignments

3.4 PCI Express Endpoint Connector

The PCI Express male connector enables access to Endpoint PCI Express components as a x1, x4, or x8 PCI Express 2.0/3.0 Link.

Figure 7: PCI Express connector

The table below describes pin assignments for the PCI Express Endpoint connector. Shaded signals are defined as optional by the *PCI Express Card Electromechanical Specification 2.0*, and signals that appear bold are active signals implemented on the XpressGX5LP-SE.

Side B			Side A		
PCI Express Pin	**FPGA Pin**	**Signal**	**PCI Express Pin**	**FPGA Pin**	**Signal**
1	--	+12V	1	connected to mPRSNT#2	mPRSNT1#
2	--	+12V	2	--	+12V
3	--	+12V	3	--	+12V
4	--	GND	4	--	GND
5	MAX2 - J8	Sm_clk	5	nc	JTAG2
6	MAX2 - H8	Sm_dat	6	nc	JTAG3
7	--	GND	7	nc	JTAG4
8	--	+3.3V	8	nc	JTAG5
9	nc	JTAG1	9	--	+3.3V
10	Linked to 3.3V via a jumper	3.3Vaux	10	--	+3.3V
11	nc	mWAKE#	11	AC28	**mPERST**#
--	--	--	--	--	--
12	--	RSVD	12	--	GND
13	--	GND	13	AF34	PCIe_CLKp
14	AV38	mPERp0	14	AF35	PCIe_CLKn
15	AV39	mPERn0	15	--	GND

Table 7: Pin assignments for the PCI Express endpoint connector

Side B			Side A		
PCI Express Pin	FPGA Pin	Signal	PCI Express Pin	FPGA Pin	Signal
16	--	GND	16	AU36	mPETp0
17	connected to mPRSNT#1	mPRSNT2#	17	AU37	mPETn0
18	--	GND	18	--	GND
19	AT38	mPERp1	19	--	RSVD
20	AT39	mPERn1	20	--	GND
21	--	GND	21	AR36	mPETp1
22	--	GND	22	AR37	mPETn1
23	AP38	mPERp2	23	--	GND
24	AP39	mPERn2	24	--	GND
25	--	GND	25	AN36	mPETp2
26	--	GND	26	AN37	mPETn2
27	AM38	mPERp3	27	--	GND
28	AM39	mPERn3	28	--	GND
29	--	GND	29	AL36	mPETp3
30	--	RSVD	30	AL37	mPETn3
31	connected to mPRSNT#1	mPRSNT#2	31	--	GND
32	--	GND	32	--	RSVD
33	AH38	mPERp4	33	--	RSVD
34	AH39	mPERn4	34	--	GND
35	--	GND	35	AG36	mPETp4
36	--	GND	36	AG37	mPETn4
37	AF38	mPERp5	37	--	GND
38	AF39	mPERn5	38	--	GND
39	--	GND	39	AE36	mPETp5
40	--	GND	40	AE37	mPETn5
41	AD38	mPERp6	41	--	GND
42	AD39	mPERn6	42	--	GND
43	--	GND	43	AC36	mPETp6
44	--	GND	44	AC37	mPETn6
45	AB38	mPERp7	45	--	GND
46	AB39	mPERn7	46	--	GND
47	--	GND	47	AA36	mPETp7

Table 7: Pin assignments for the PCI Express endpoint connector

Side B			Side A		
PCI Express Pin	FPGA Pin	Signal	PCI Express Pin	FPGA Pin	Signal
48	connected to mPRSNT#1	mPRSNT#2	48	AA37	mPETn7
49	--	GND	49	--	GND

Table 7: Pin assignments for the PCI Express endpoint connector

3.5 QDR2+ SRAM

The XpressGX5LP-SE features two independent banks of QDR2+ SRAM, each capable of addressing up to 144Mbit in an 18-bit wide datapath. The two mounted devices are GSI G581302DT20GE-450..

Figure 8: QDR2+ SRAM

The following table shows pin assignments for the QDR2+ SRAM:

Bank 0		Bank 1	
FPGA Pin	Signal	FPGA Pin	Signal
QDR2a_a00	U14	QDR2b_a00	T12
QDR2a_a01	P14	QDR2b_a01	K12
QDR2a_a02	J15	QDR2b_a02	K13
QDR2a_a03	T13	QDR2b_a03	N13
QDR2a_a04	R14	QDR2b_a04	M12
QDR2a_a05	R12	QDR2b_a05	L12
QDR2a_a06	P13	QDR2b_a06	L13
QDR2a_a07	J14	QDR2b_a07	J12
QDR2a_a08	H14	QDR2b_a08	J13
QDR2a_a09	A14	QDR2b_a09	D12

Table 8: QDR2+ SRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
QDR2a_a10	G15	QDR2b_a10	G12
QDR2a_a11	G14	QDR2b_a11	H13
QDR2a_a12	B14	QDR2b_a12	C12
QDR2a_a13	C15	QDR2b_a13	D13
QDR2a_a14	F14	QDR2b_a14	G13
QDR2a_a15	C14	QDR2b_a15	E12
QDR2a_a16	E14	QDR2b_a16	F12
QDR2a_a17	D15	QDR2b_a17	C13
QDR2a_a18	E15	QDR2b_a18	A13
QDR2a_a19	F15	QDR2b_a19	B13
QDR2a_a20	U12	QDR2b_a20	U11
QDR2a_a21	U13	QDR2b_a21	N12
QDR2a_bws0	L18	QDR2b_bws0	N9
QDR2a_bws1	K19	QDR2b_bws1	N8
QDR2a_CKn	F18	QDR2b_CKn	C9
QDR2a_CKp	G18	QDR2b_CKp	C8
QDR2a_CQn	P16	QDR2b_CQn	M11
QDR2a_CQp	H16	QDR2b_CQp	B10
QDR2a_d00	D18	QDR2b_d00	E9
QDR2a_d01	D19	QDR2b_d01	G10
QDR2a_d02	C18	QDR2b_d02	D9
QDR2a_d03	C19	QDR2b_d03	E8
QDR2a_d04	B19	QDR2b_d04	F9
QDR2a_d05	A19	QDR2b_d05	B8
QDR2a_d06	G19	QDR2b_d06	A8
QDR2a_d07	H19	QDR2b_d07	J9
QDR2a_d08	L19	QDR2b_d08	K9
QDR2a_d09	N19	QDR2b_d09	L9
QDR2a_d10	N18	QDR2b_d10	M8
QDR2a_d11	N17	QDR2b_d11	M9
QDR2a_d12	P17	QDR2b_d12	T9
QDR2a_d13	R16	QDR2b_d13	R9
QDR2a_d14	M17	QDR2b_d14	L8

Table 8: QDR2+ SRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
QDR2a_d15	K18	QDR2b_d15	G9
QDR2a_d16	M18	QDR2b_d16	G8
QDR2a_d17	J18	QDR2b_d17	F8
QDR2a_Doff	K15	QDR2b_Doff	D6
QDR2a_q00	E17	QDR2b_q00	A10
QDR2a_q01	A17	QDR2b_q01	A11
QDR2a_q02	B17	QDR2b_q02	B11
QDR2a_q03	A16	QDR2b_q03	C10
QDR2a_q04	B16	QDR2b_q04	D10
QDR2a_q05	C16	QDR2b_q05	H11
QDR2a_q06	D16	QDR2b_q06	J11
QDR2a_q07	F17	QDR2b_q07	K10
QDR2a_q08	G16	QDR2b_q08	N10
QDR2a_q09	U15	QDR2b_q09	U10
QDR2a_q10	T15	QDR2b_q10	U9
QDR2a_q11	T16	QDR2b_q11	R10
QDR2a_q12	R15	QDR2b_q12	T10
QDR2a_q13	N16	QDR2b_q13	P10
QDR2a_q14	M15	QDR2b_q14	H10
QDR2a_q15	N15	QDR2b_q15	J10
QDR2a_q16	H17	QDR2b_q16	F11
QDR2a_q17	G17	QDR2b_q17	E11
QDR2a_QVLD	L15	QDR2b_QVLD	E7
QDR2a_rps	M14	QDR2b_rps	E6
QDR2a_wps	N14	QDR2b_wps	F6

Table 8: QDR2+ SRAM pin assignments

3.6 DDR3L SDRAM

The XpressGX5LP-SE features 2 independent banks of DDR3L SDRAM, each capable of addressing 4 GB in a 72-bit wide datapath. The 18 mounted devices are Micron MT41K512M8RA-125.

Figure 9: DDR3L SDRAM

The following table shows pin assignments for the DDR3L SDRAM:

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_a00	AM17	ddr3_Bank1_a00	C22
ddr3_Bank0_a01	AR18	ddr3_Bank1_a01	E20
ddr3_Bank0_a02	AF16	ddr3_Bank1_a02	E23
ddr3_Bank0_a03	AM16	ddr3_Bank1_a03	A23
ddr3_Bank0_a04	AR19	ddr3_Bank1_a04	G20
ddr3_Bank0_a05	AG16	ddr3_Bank1_a05	F23
ddr3_Bank0_a06	AP19	ddr3_Bank1_a06	K22
ddr3_Bank0_a07	AW17	ddr3_Bank1_a07	G23
ddr3_Bank0_a08	AM19	ddr3_Bank1_a08	K21
ddr3_Bank0_a09	AT17	ddr3_Bank1_a09	D21
ddr3_Bank0_a10	AT18	ddr3_Bank1_a10	F20
ddr3_Bank0_a11	AP18	ddr3_Bank1_a11	J22
ddr3_Bank0_a12	AU18	ddr3_Bank1_a12	F21
ddr3_Bank0_a13	AW16	ddr3_Bank1_a13	E21
ddr3_Bank0_a14	AV17	ddr3_Bank1_a14	J21
ddr3_Bank0_a15	AL18	ddr3_Bank1_a15	G22
ddr3_Bank0_ba0	AL16	ddr3_Bank1_ba0	B23

Table 9: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_ba1	AV19	ddr3_Bank1_ba1	G21
ddr3_Bank0_ba2	AU16	ddr3_Bank1_ba2	B20
ddr3_Bank0_cas#	AR17	ddr3_Bank1_cas#	D22
ddr3_Bank0_cke0	AW19	ddr3_Bank1_cke0	H20
ddr3_Bank0_cke1	AN8	ddr3_Bank1_cke1	H22
ddr3_Bank0_CKn	AN18	ddr3_Bank1_CKn	N21
ddr3_Bank0_CKp	AN19	ddr3_Bank1_CKp	N20
ddr3_Bank0_cs0#	AN17	ddr3_Bank1_cs0#	K24
ddr3_Bank0_cs1#	AJ6	ddr3_Bank1_cs1#	H23
ddr3_Bank0_d00	AJ15	ddr3_Bank1_d00	C24
ddr3_Bank0_d01	AG14	ddr3_Bank1_d01	C25
ddr3_Bank0_d02	AB16	ddr3_Bank1_d02	G24
ddr3_Bank0_d03	AB15	ddr3_Bank1_d03	D25
ddr3_Bank0_d04	AH15	ddr3_Bank1_d04	D24
ddr3_Bank0_d05	AG15	ddr3_Bank1_d05	F24
ddr3_Bank0_d06	AD16	ddr3_Bank1_d06	H25
ddr3_Bank0_d07	AC15	ddr3_Bank1_d07	G25
ddr3_Bank0_d08	AH19	ddr3_Bank1_d08	J25
ddr3_Bank0_d09	AJ18	ddr3_Bank1_d09	P26
ddr3_Bank0_d10	AE18	ddr3_Bank1_d10	K25
ddr3_Bank0_d11	AK18	ddr3_Bank1_d11	P25
ddr3_Bank0_d12	AG19	ddr3_Bank1_d12	M26
ddr3_Bank0_d13	AJ19	ddr3_Bank1_d13	N25
ddr3_Bank0_d14	AE19	ddr3_Bank1_d14	L26
ddr3_Bank0_d15	AH18	ddr3_Bank1_d15	N26
ddr3_Bank0_d16	AE9	ddr3_Bank1_d16	H26
ddr3_Bank0_d17	AC10	ddr3_Bank1_d17	C26
ddr3_Bank0_d18	AC9	ddr3_Bank1_d18	J26
ddr3_Bank0_d19	AB10	ddr3_Bank1_d19	C27
ddr3_Bank0_d20	AD9	ddr3_Bank1_d20	F26
ddr3_Bank0_d21	AJ10	ddr3_Bank1_d21	D27
ddr3_Bank0_d22	AB9	ddr3_Bank1_d22	G26
ddr3_Bank0_d23	AH10	ddr3_Bank1_d23	E27

Table 9: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_d24	AU9	ddr3_Bank1_d24	K27
ddr3_Bank0_d25	AM10	ddr3_Bank1_d25	R27
ddr3_Bank0_d26	AT9	ddr3_Bank1_d26	M27
ddr3_Bank0_d27	AL10	ddr3_Bank1_d27	T27
ddr3_Bank0_d28	AP9	ddr3_Bank1_d28	P28
ddr3_Bank0_d29	AR9	ddr3_Bank1_d29	J27
ddr3_Bank0_d30	AU10	ddr3_Bank1_d30	N27
ddr3_Bank0_d31	AN9	ddr3_Bank1_d31	L27
ddr3_Bank0_d32	AA12	ddr3_Bank1_d32	D30
ddr3_Bank0_d33	AD14	ddr3_Bank1_d33	H31
ddr3_Bank0_d34	AA13	ddr3_Bank1_d34	F30
ddr3_Bank0_d35	AH13	ddr3_Bank1_d35	E31
ddr3_Bank0_d36	AC13	ddr3_Bank1_d36	E30
ddr3_Bank0_d37	AJ13	ddr3_Bank1_d37	G31
ddr3_Bank0_d38	AB13	ddr3_Bank1_d38	G30
ddr3_Bank0_d39	AC14	ddr3_Bank1_d39	C30
ddr3_Bank0_d40	AV14	ddr3_Bank1_d40	N30
ddr3_Bank0_d41	AP13	ddr3_Bank1_d41	L30
ddr3_Bank0_d42	AV13	ddr3_Bank1_d42	R31
ddr3_Bank0_d43	AN13	ddr3_Bank1_d43	K30
ddr3_Bank0_d44	AW14	ddr3_Bank1_d44	M30
ddr3_Bank0_d45	AL13	ddr3_Bank1_d45	J30
ddr3_Bank0_d46	AW13	ddr3_Bank1_d46	R30
ddr3_Bank0_d47	AM13	ddr3_Bank1_d47	L31
ddr3_Bank0_d48	AR14	ddr3_Bank1_d48	J28
ddr3_Bank0_d49	AR15	ddr3_Bank1_d49	P29
ddr3_Bank0_d50	AM14	ddr3_Bank1_d50	J29
ddr3_Bank0_d51	AK14	ddr3_Bank1_d51	R29
ddr3_Bank0_d52	AN14	ddr3_Bank1_d52	L28
ddr3_Bank0_d53	AT15	ddr3_Bank1_d53	V29
ddr3_Bank0_d54	AL14	ddr3_Bank1_d54	K28
ddr3_Bank0_d55	AU15	ddr3_Bank1_d55	U29
ddr3_Bank0_d56	AK12	ddr3_Bank1_d56	E28
ddr3_Bank0_d57	AE11	ddr3_Bank1_d57	C28

Table 9: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_d58	AG12	ddr3_Bank1_d58	D28
ddr3_Bank0_d59	AD12	ddr3_Bank1_d59	A28
ddr3_Bank0_d60	AF11	ddr3_Bank1_d60	F29
ddr3_Bank0_d61	AE10	ddr3_Bank1_d61	B29
ddr3_Bank0_d62	AL12	ddr3_Bank1_d62	B28
ddr3_Bank0_d63	AE12	ddr3_Bank1_d63	A29
ddr3_Bank0_d64	AV11	ddr3_Bank1_d64	G34
ddr3_Bank0_d65	AR11	ddr3_Bank1_d65	E32
ddr3_Bank0_d66	AK11	ddr3_Bank1_d66	H34
ddr3_Bank0_d67	AL11	ddr3_Bank1_d67	F32
ddr3_Bank0_d68	AW11	ddr3_Bank1_d68	K33
ddr3_Bank0_d69	AT11	ddr3_Bank1_d69	J34
ddr3_Bank0_d70	AR12	ddr3_Bank1_d70	J33
ddr3_Bank0_d71	AU11	ddr3_Bank1_d71	K34
ddr3_Bank0_dqs00n	AE15	ddr3_Bank1_dqs00n	E25
ddr3_Bank0_dqs00p	AD15	ddr3_Bank1_dqs00p	E24
ddr3_Bank0_dqs01n	AG18	ddr3_Bank1_dqs01n	R26
ddr3_Bank0_dqs01p	AF19	ddr3_Bank1_dqs01p	R25
ddr3_Bank0_dqs02n	AG10	ddr3_Bank1_dqs02n	F27
ddr3_Bank0_dqs02p	AF10	ddr3_Bank1_dqs02p	G27
ddr3_Bank0_dqs03n	AW10	ddr3_Bank1_dqs03n	T28
ddr3_Bank0_dqs03p	AV10	ddr3_Bank1_dqs03p	U28
ddr3_Bank0_dqs04n	AF14	ddr3_Bank1_dqs04n	C31
ddr3_Bank0_dqs04p	AE14	ddr3_Bank1_dqs04p	D31
ddr3_Bank0_dqs05n	AU14	ddr3_Bank1_dqs05n	N31
ddr3_Bank0_dqs05p	AT14	ddr3_Bank1_dqs05p	P31
ddr3_Bank0_dqs06n	AP15	ddr3_Bank1_dqs06n	T30
ddr3_Bank0_dqs06p	AN15	ddr3_Bank1_dqs06p	U30
ddr3_Bank0_dqs07n	AJ12	ddr3_Bank1_dqs07n	G29
ddr3_Bank0_dqs07p	AH12	ddr3_Bank1_dqs07p	H29
ddr3_Bank0_dqs08n	AU12	ddr3_Bank1_dqs08n	E33
ddr3_Bank0_dqs08p	AT12	ddr3_Bank1_dqs08p	F33
ddr3_Bank0_odt0	AN16	ddr3_Bank1_odt0	A22
ddr3_Bank0_odt1	AJ7	ddr3_Bank1_odt1	B22

Table 9: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_ras#	AV16	ddr3_Bank1_ras#	C21
ddr3_Bank0_rst#	AU17	ddr3_Bank1_rst#	C20
ddr3_Bank0_tdqs00n	AA15	ddr3_Bank1_tdqs00n	A25
ddr3_Bank0_tdqs00p	AA14	ddr3_Bank1_tdqs00p	B25
ddr3_Bank0_tdqs01n	AD17	ddr3_Bank1_tdqs01n	T25
ddr3_Bank0_tdqs01p	AD18	ddr3_Bank1_tdqs01p	U25
ddr3_Bank0_tdqs02n	AH9	ddr3_Bank1_tdqs02n	A26
ddr3_Bank0_tdqs02p	AG9	ddr3_Bank1_tdqs02p	B26
ddr3_Bank0_tdqs03n	AP10	ddr3_Bank1_tdqs03n	U27
ddr3_Bank0_tdqs03p	AN10	ddr3_Bank1_tdqs03p	U26
ddr3_Bank0_tdqs04n	AG13	ddr3_Bank1_tdqs04n	A31
ddr3_Bank0_tdqs04p	AF13	ddr3_Bank1_tdqs04p	B31
ddr3_Bank0_tdqs05n	AP12	ddr3_Bank1_tdqs05n	J31
ddr3_Bank0_tdqs05p	AN12	ddr3_Bank1_tdqs05p	K31
ddr3_Bank0_tdqs06n	AL15	ddr3_Bank1_tdqs06n	M29
ddr3_Bank0_tdqs06p	AK15	ddr3_Bank1_tdqs06p	N28
ddr3_Bank0_tdqs07n	AC12	ddr3_Bank1_tdqs07n	G28
ddr3_Bank0_tdqs07p	AB12	ddr3_Bank1_tdqs07p	H28
ddr3_Bank0_tdqs08n	AN11	ddr3_Bank1_tdqs08n	G32
ddr3_Bank0_tdqs08p	AM11	ddr3_Bank1_tdqs08p	G33
ddr3_Bank0_we#	AP16	ddr3_Bank1_we#	A20

Table 9: DDR3L SDRAM pin assignments

3.7 Dual SFP+ Interface

The XpressGX5LP-SE dual SFP+ interfaces uses FPGA GXB transceivers to enable two optical links. Each transmitter can be driven by its SFPX_SUPPLY_EN active-low control signal. An SFPX_SUPPLY_FAULT fault signal is available in case of overload on transmitters..

Figure 10: QSFP+ interface

The XpressGX5LP-SE Dual SFP+ interface uses FPGA GXB transceivers to enable two 1/10 Gbit Ethernet links:

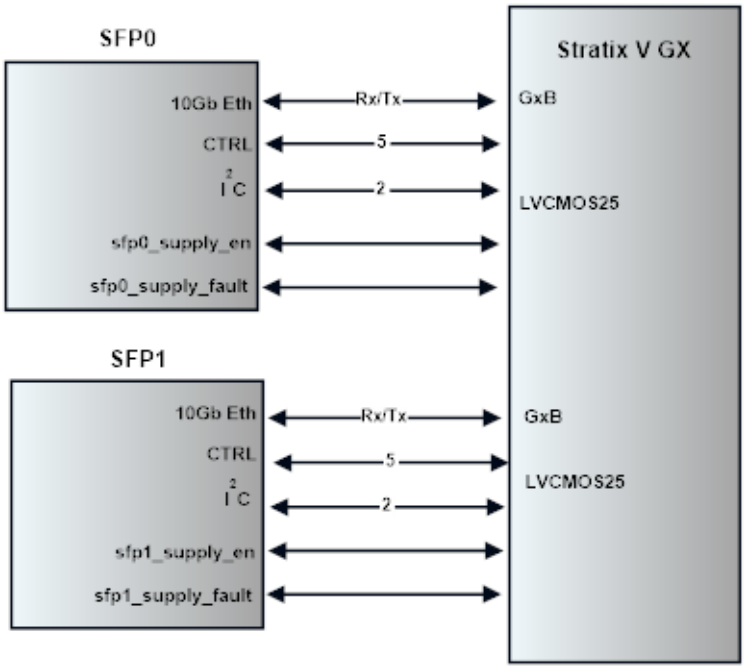

Figure 11: 10/1 Gbs links using the Dual SFP+ interface

The following table shows the QSFP+ pin assignments on the FPGA:

SFP1	FPGA Pin	SFP2	FPGA Pin
sfp0_frxip_n	AT2	sfp1_frxip_n	AV2
sfp0_frxip_p	AT1	sfp1_frxip_p	AV1
sfp0_ftxout_n	AR3	sfp1_ftxout_n	AU3
sfp0_ftxout_p	AR4	sfp1_ftxout_p	AU4
sfp0_gpio3_0	AJ21	sfp1_gpio3_0	AG23
sfp0_gpio3_1	AT20	sfp1_gpio3_1	AG25
sfp0_mod_abs	AH21	sfp1_mod_abs	AJ24
sfp0_rx_los	AP21	sfp1_rx_los	AH25
sfp0_tx_disable	AD20	sfp1_tx_disable	AG22
sfp0_tx_fault	AD21	sfp1_tx_fault	AG21
sfp0_supply_fault	AT21	sfp1_supply_fault	AP22
sfp0_supply_en	AR21	sfp1_supply_en	AN22
sfp0_uc_scl	AE20	sfp1_uc_scl	AK24
sfp0_uc_sda	AE21	sfp1_uc_sda	AL24

Table 10: SFP+ pin assignments

Note: Each SFP+ Transmitter supply is driven by the `SFPX_SUPPLY_EN` active-low control signal. These signals must be set to '0' to enable SFPx supplies.

3.8 Dual Tri-Color LEDs

The XpressGX5LP-SE features two dual tri-color (Green/Red/Amber) LEDs on each side of the two SFP+ connectors. These LEDs can be used to display SFP+ information, and can also be used for user-defined purposes.

LED	Green LED	FPGA Pin	Red LED	FPGA Pin
LED SFP0_1	sfp0_led_g1	AW20	sfp0_led_r1	AU20
LED SFP0_2	sfp0_led_g2	AV20	sfp0_led_r2	AH27
LED_SFP1_1	sfp1_led_g1	AN23	sfp1_led_r1	AL22
LED_SFP1_2	sfp1_led_g2	AM22	sfp1_led_r2	AG27

Table 11: Dual tri-color LED pin assignments

Each LED consists of one green LED and one red LED. If both are on, then the LED will glow amber.

3.9 LEDs

Eight user LEDs are available on the board:

Figure 12: User LEDs

The following table describes pin assignments for the LEDs:

Signal	FPGA Pin	LED Name	LED Color
user_led0	AJ20	DS2	Yellow
user_led1	AK21	DS3	Yellow
user_led2	AL20	DS4	Green
user_led3	AL21	DS5	Green
user_led4	AM20	DS6	Orange
user_led5	AN21	DS7	Orange
user_led6	AN20	DS8	Red
user_led7	AR20	DS9	Red

Table 12: Pin assignments for the board LEDs

3.10 Local Reset

One active low reset push button is available on the board to enable register initialization:

Figure 13: Reset button

Signal	FPGA Pin
user_resetn	C7

Table 13: Pin assignments for the reset button

3.11 Mechanical Switches

Three user switches are available on the solder side of the XpressGX5LP-SE on SW1. These enable three IOs to be set to a logical ’0’ or a logical ’1’. A fourth switch (SW1-4) enables you to select the configuration bit stream to load on the FPGA during configuration. This switch is not connected to the FPGA.

Figure 14: Mechanical switches

Signal Name	FPGA Pin or Function	Module
user_sw_a	B7	SW1-1
user_sw_b	A7	SW1-2

Table 14: Pin assignments for the mechanical switches

Signal Name	FPGA Pin or Function	Module
user_sw_c	D7	SW1-3
max_sw0	Configuration boot selection/ config MAX pin_A10	SW1-4

Table 14: Pin assignments for the mechanical switches

3.12 EEPROMs

Two 256k-bit Serial FlashPROMs (M24256BSMN6T) are available on the solder side of the XpressGX5LP for data storage via two I²C links.

The following table shows pin assignments for the EEPROMs:

EEPROM 0 Signal	FPGA Pin	EEPROM 1Signal	FPGA Pin
eeprom0_scl	J7	eeprom1_scl	K6
eeprom0_sda	K7	eeprom1_sda	G7
eeprom0_wr	H7	eeprom1_wr	G6

Table 15: Pin assignments for the EEPROMs

3.13 Power Supply

The XpressGX5LP-SE board is supplied by both the 12 V and 3.3 V of the PCI Express slot. These voltages are available on the mezzanine power supply daughter card, which is mounted on the XpressGX5LP-SE by default.

The PCI Express 12 V generates 1.5 V, 1.8 V, 2.5 V, and 0.9 V voltages, while the 3.3 V generates 3.0 V voltages, as shown below.

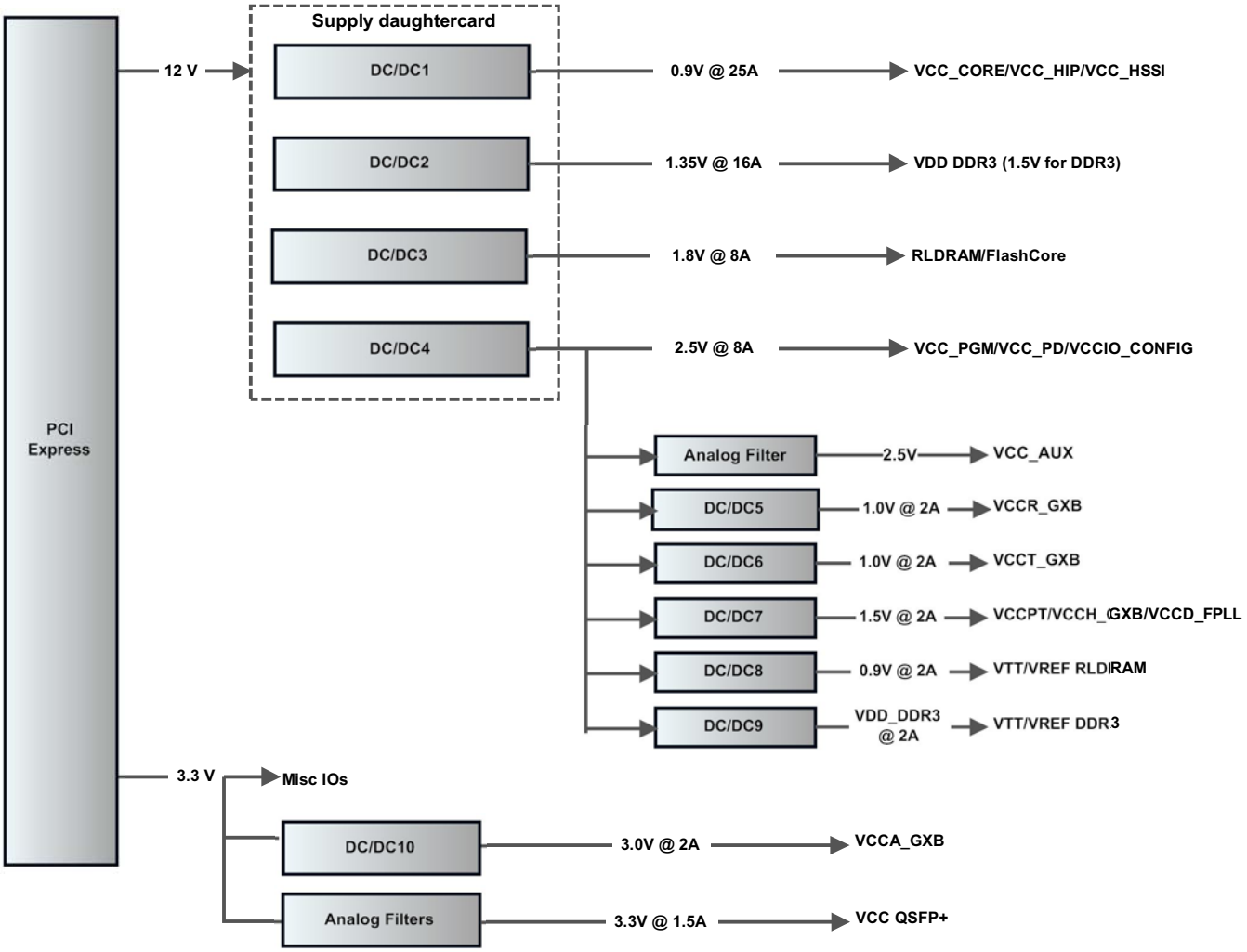

Figure 15: Power Distribution for the XpressGX5LP-SE

Note: The figures above are provided for illustrative purposes only.