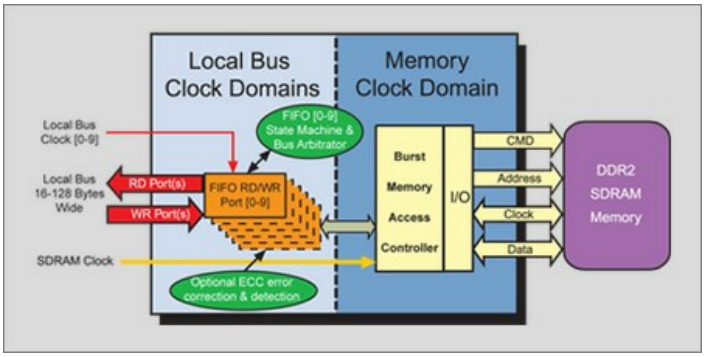
FPGA IP Core Development Solutions

Our FPGA offerings include development boards and IP cores for Altera FPGA devices. The IP cores include: I2C, PCIe, JPEG-LS, LVDS Camera Link and memory controllers.

Avalon Multi-port DDR2 Memory Controller IP Core



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Key Features

- 200 / 333 MHz (400/666 Mbps) Cyclone/Stratix DDR2 memory performance
- DDR2 Memory Devices
- From 1 to 16 Avalon-MM local bus port interfaces
- Memory bandwidth utilization in excess of 95%
- Avalon Pipelined and Burst transfers
- Avalon local bus width from 8 to 128-bits
- Memory data width: 8/16/32/64-bit
- Configurable FIFO depth: 16 to 2048 bytes
- Intelligent SDRAM burst caching controller minimizes wait-states
- PCB layout independent DDR2 Round-Trip capture scheme
- Requires only single PLL with 2 clock outputs
- Independent system/memory time domain clocking
- Supports: Cyclone II, III, IV-E, IV-GX, V, Stratix II, II-GX, III, IV/IV-GX and Arria GX/II-GX

Memory Performance Chart

DDR2 MEMORY PERFORMANCE

Device	Speed Grade (Commercial)	MHz
Arria II GX	-6, -5, -4	200, 233, 267
Arria GX	-6	200
Stratix IV/GX	-4, -3, -2	267, 300, 333
Stratix III	-5, -4, -3	233, 267, 300
Stratix II/GX	-5, -4, -3	233, 267, 300
Cyclone IV E	-9L, -8L, -7L	133, 167, 200
Cyclone III	-8, -7, -6	160, 167, 200
Cyclone II	-8, -7, -6	160, 180, 200

Overview

The Microtronix Avalon Multi-port DDR2 Memory Controller IP Core is designed for maximizing the performance of an Altera Nios II processor in Avalon® multi-master streaming data systems. Advanced design features enable maximum system clock rates using low speed FPGA's and standard memory devices, lowering your production cost, and saving you money.

The Avalon-MM slave ports can be independently clocked allowing the system to be partitioned and optimized to achieve maximum performance. Supporting post memory read and write cycles, the data FIFO's effectively double

Additional Images

Ordering Information

Part Number: 5240-01-04

MSRP: $3,250.00 USD

Floating Server License (Optional Upgrade)

- 1 Seat $0
- 2 Seat $500
- 5 Seat $750

Add to Cart

Options

- 2 Hour Technical Support Contract

memory bandwidth on sequential address or FIFO cache hits. FIFO depth can be tailored for either streaming or random access.

The core is optimized for Altera® Cyclone, Arria and Stratix device families of field programmable logic devices. The Avalon Slave ports are configured with Qsys GUI which greatly simplifies the design of Avalon-MM based SOC systems.

The DDR2 Memory Controller handles all memory tasks, including initialization and refresh cycles. It is designed to operate asynchronous to the local port clocks enabling the memory to be clocked at its peaked rated frequency maximizing system performance.

IP Core Advantages

- MegaWizzard GUI for ease of configuration
- Requires only single PLL with 2 clock outputs
- DQS data capture clocking simplifies DDR2 PCB constraints and eliminates dedicated data capture PLL
- Configurable FIFO maximizes performance of streaming data applications
- Configurable memory and local bus data width optimizes cost
- Independent time domain clocking optimizes memory bandwidth
- Round-robin (dafault) and user configurable bus arbitration schemes
- Synopsis TimeQuest support ensures timing closure

Other Features

- Altera Qsys Configuration GUI
- Supports Synopsys TimeQuest timing analyzer
- VHDL IP functional simulations models
- On Die Termination (ODT) improves signal integrity
- Altera OpenCore Plus evaluation

License Options

- Node Locked: Supports a single user. It is tied to NIC ID (MAC address) of a PC.
- Floating Server: Supports multiple users, typically 1, 2 or 5 seats

NOTE: The Base IP Core license supports a single FPGA device family. Licenses supporting multiple FPGA device families are available. Contact sales for more information.

Custom Core

The IP Core can be customized for additional bus ports or for wider data widths. Contact sales with your requirements.

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